CLAIMS

What is claimed is:

1. A non-volatile memory comprising:

a chalcogenide storage element;

a voltage limiting circuit, coupled to said chalcogenide storage element, for ensuring that voltages across said chalcogenide storage element do not exceed a predetermined value during a read operation;

a current-to-voltage converter circuit, coupled to said voltage limiting circuit, for converting a current pulse read from said chalcogenide storage element to a voltage pulse during said read operation; and

a buffer circuit, coupled to said current-to-voltage converter circuit, for sensing said voltage pulse to determine a storage phase of said chalcogenide storage element during said read operation.

2. The non-volatile memory of Claim 1, wherein said current-to-voltage converter circuit includes a p-channel transistor, an n-channel transistor and an inverter.

3. The non-volatile memory of Claim 1, wherein said chalcogenide storage element is capable of changing from an amorphous phase to a crystalline phase, or vice versa, via an application of an appropriate amount of current.

4. The non-volatile memory of Claim 3, wherein current for said chalcogenide storage element to reach said amorphous phase and said crystalline phase are 1 mA and 0.5 mA, respectively.

5. The non-volatile memory of Claim 1, wherein said non-volatile memory further includes a row decoder circuit for receiving an address input and a clock input.

6. A write circuit for writing data to a non-volatile memory, said write circuit comprising:

a chalcogenide storage element;

a write control circuit for receiving a write_enable input, a col_write input and a data_in input;

a row decoder circuit, coupled to said chalcogenide storage element, for receiving an address input and a clock input; and

a write current supply circuit, coupled to said write control circuit and said chalcogenide storage element, for writing data to said chalcogenide storage element during a write operation under the control of said write control circuit.

7. The write circuit of Claim 6, wherein said write current supply circuit includes two p-channel transistors.

8. The write circuit of Claim 6, wherein said chalcogenide storage element is capable of changing from an amorphous phase to a crystalline phase, or vice versa, via an application of an appropriate amount of current.

9. The write circuit of Claim 8, wherein current for said chalcogenide storage element to reach said amorphous phase and said crystalline phase are 1 mA and 0.5 mA, respectively.

10. A read circuit for reading data from a non-volatile memory, said read circuit comprising:

a chalcogenide storage element;

a read control circuit for receiving a read_enable input, an address_column input to generate a column_read signal;

a row decoder circuit, coupled to said chalcogenide storage element, for receiving an address input and a clock input; and

a current-to-voltage circuit, coupled to said read control circuit and said chalcogenide storage element, for sensing a current flowing through said chalcogenide storage element during a read operation under the control of said read control circuit.

11. The read circuit of Claim 10, wherein said current-to-voltage circuit includes a p-channel transistor, an n-channel transistor and an inverter.

12. The read circuit of Claim 10, wherein said chalcogenide storage element is capable of changing from an amorphous phase to a crystalline phase, or vice versa, via an application of an appropriate amount of current.

13. The read circuit of Claim 12, wherein said flow-through current is 1 mA and 0.5 mA when said chalcogenide storage element is in said amorphous phase and said crystalline phase, respectively.

14. The read circuit of Claim 10, wherein said read circuit further includes a buffer for buffering output voltages from said current-to-voltage converter circuit.